WHAT IS CLAIMED IS:

1. A semiconductor device for driving liquid crystals comprising:

a single-port memory that stores display-data to be displayed on a liquid crystal displaying section;

a liquid crystal driver that retrieves the display-data stored in the single-port memory on a specific cycle and sends the display-data to the liquid crystal displaying section; and

a controller that controls the liquid crystal driver so that, when a CPU does not have access to the single-port memory, the display-data is retrieved from the single-port memory to the liquid crystal driver on the specific cycle and the retrieved data is sent to the liquid crystal displaying section, whereas, when the CPU has access to the single-port memory while the data is being retrieved from the single-port memory to the liquid crystal driver, a priority is given to the CPU so that the CPU starts an access operation while the liquid crystal driver stops a display-data retrieval operation, and on completion of the access operation, the liquid crystal driver starts again the display-data retrieval operation.

2. The semiconductor device for driving liquid crystals according to claim 1, wherein the controller controls the liquid crystal driver so that the liquid crystal driver stops the display-data retrieval operation when a display-data retrieval timing comes while the CPU is having access to the single-port memory, and on completion of the access operation, the liquid crystal driver starts the display-data retrieval operation.

3. The semiconductor device for driving liquid crystals according to claim 1, wherein the liquid crystal driver includes:

a first latch circuit that stores the display-data from the single-port memory in response to a first latch signal; and

a second latch circuit that stores an output of the first latch circuit in response to a second latch signal,

and wherein the controller outputs the first latch signal

based on the second latch signal and a CPU-access signal that indicates the access operation of the CPU to the single-port memory.

4. The semiconductor device for driving liquid crystals according to claim 3, wherein the first and the second latch circuits are provided for each output port of the single-port memory.

5. The semiconductor device for driving liquid crystals according to claim 3, wherein the controller includes a delay circuit, and controls the liquid crystal driver so that, when the second latch signal is activated while the CPU does not have access to the single-port memory, a pulse signal is output as the first latch signal in synchronism with the activation of the second latch signal for a period corresponding to a delay time of the delay circuit, and then the output of the first latch circuit is stored in the second latch circuit when the second latch signal is deactivated.

6. The semiconductor device for driving liquid crystals according to claim 3, wherein the controller includes a delay circuit, and controls the liquid crystal driver so that, when the second latch signal is activated while the CPU is having access to the single-port memory, the access to the single-port memory is prioritized, a pulse signal is output as the first latch signal for a period corresponding to a delay time of the delay circuit on completion of the access operation, and then the output of the first latch circuit is stored in the second latch circuit when the second latch signal is deactivated.

7. The semiconductor device for driving liquid crystals according to claim 3, wherein the controller includes a delay circuit, and controls the liquid crystal driver so that, when the CPU starts to have access to the single-port memory while the first latch signal is being output in synchronism with activation of the second latch signal, the access to the

single-port memory is prioritized while a latching operation of the first latch circuit is halted, a pulse signal is output again as the first latch signal for a period corresponding to a delay time of the delay circuit on completion of the access operation, and then the output of the first latch circuit is stored in the second latch circuit when the second latch signal is deactivated.

8. The semiconductor device for driving liquid crystals according to claim 3, wherein the controller includes a delay circuit, and controls the liquid crystal driver so that, when the CPU starts the access operation after a pulse signal has been output as the first latch signal for a period corresponding to a delay time of the delay circuit in response to activation of the second latch signal, while the second latch signal has still been activated, the access operation is performed whereas the first latch signal is not output again on completion of the access operation, and then the output of the first latch circuit is stored in the second latch circuit when the second latch signal is deactivated.

9. The semiconductor device for driving liquid crystals according to claim 3, wherein a pulse width for the CPU-access signal is narrower than a difference between a pulse width for the second latch signal and the delay time of the delay circuit.

10. A semiconductor device for driving liquid crystals comprising:

a single-port memory that stores display-data to be displayed on a liquid crystal displaying section;

a liquid crystal driver, having a latch circuit that stores the display-data stored in the single-port memory, that retrieves the display-data from the single-port memory on a specific cycle and sends the display-data to the liquid crystal displaying section; and

a controller that generates a latch control signal and sends the latch control signal to the latch circuit, the latch control signal being generated based on a CPU-access signal

indicating an access operation of a CPU to the single-port memory and a specific signal that is synchronized with a display-data retrieval cycle for the liquid crystal driver.

11. The semiconductor device for driving liquid crystals according to claim 10, wherein the liquid crystal driver includes:

a first latch circuit that stores the display-data from the single-port memory in response to a first latch signal; and

a second latch circuit that stores an output of the first latch circuit in response to a second latch signal,

and wherein the controller outputs the first latch signal based on the CPU-access signal and the second latch signal.

12. The semiconductor device for driving liquid crystals according to claim 11, wherein the first and the second latch circuits are provided for each output port of the single-port memory.

13. The semiconductor device for driving liquid crystals according to claim 11, wherein the controller includes a delay circuit, and controls the liquid crystal driver so that, when the second latch signal is activated while the CPU does not have access to the single-port memory, a pulse signal is output as the first latch signal in synchronism with the activation of the second latch signal for a period corresponding to a delay time of the delay circuit, and then the output of the first latch circuit is stored in the second latch circuit when the second latch signal is deactivated.

14. The semiconductor device for driving liquid crystals according to claim 11, wherein the controller includes a delay circuit, and controls the liquid crystal driver so that, when the second latch signal is activated while the CPU is having access to the single-port memory, the access to the single-port memory is prioritized, a pulse signal is output as the first latch signal for a period corresponding to a delay time of the delay circuit on completion of the access operation, and then the output of

the first latch circuit is stored in the second latch circuit when the second latch signal is deactivated.

15. The semiconductor device for driving liquid crystals according to claim 11, wherein the controller includes a delay circuit, and controls the liquid crystal driver so that, when the CPU starts to have access to the single-port memory while the first latch signal is being output in synchronism with activation of the second latch signal, the access to the single-port memory is prioritized while a latching operation of the first latch circuit is halted, a pulse signal is output again as the first latch signal for a period corresponding to a delay time of the delay circuit on completion of the access operation, and then the output of the first latch circuit is stored in the second latch circuit when the second latch signal is deactivated.

16. The semiconductor device for driving liquid crystals according to claim 11, wherein the controller includes a delay circuit, and controls the liquid crystal driver so that, when the CPU starts the access operation after a pulse signal has been output as the first latch signal for a period corresponding to a delay time of the delay circuit in response to activation of the second latch signal, while the second latch signal has still been activated, the access operation is performed whereas the first latch signal is not output again on completion of the access operation, and then the output of the first latch circuit is stored in the second latch circuit when the second latch signal is deactivated.

17. The semiconductor device for driving liquid crystals according to claim 11, wherein a pulse width for the CPU-access signal is narrower than a difference between a pulse width for the second latch signal and the delay time of the delay circuit.

18. The semiconductor device for driving liquid crystals according to claim 11, wherein the controller includes:

a first 3-input NOR gate and a second 3-input NOR gate each

having three input terminals, each accepting an inverted signal of the second latch signal at one of the three input terminals and accepting the CPU-access signal at either of the remaining two input terminals;

a first R-S flip-flop having a set terminal and a reset terminal, that accepts an inverted signal of an output of the first 3-input NOR gate at the set terminal and an output of the second 3-input NOR gate at the reset terminal;

a delay circuit that delays an output of the first R-S flip-flop by a predetermined period;

a third 3-input NOR gate that accepts an output of the first R-S flip-flop, an inverted signal of an output of the delay circuit and the CPU-access signal; and

a second R-S flip-flop having a set terminal and a reset terminal, that accepts an inverted signal of an output of the third 3-input NOR gate at the set terminal and the second latch signal at the reset terminal,

and wherein the first 3-input NOR gate accepts the output of the second R-S flip-flop at the other of the remaining two input terminals, the second 3-input NOR gate accepts the output of the delay circuit at the other of the remaining two input terminals, and the first latch signal is output from an output terminal of the first R-S flip-flop.

19. A liquid crystal display apparatus having a semiconductor device for driving liquid crystals and a liquid crystal displaying section, the device comprising:

a single-port memory that stores display-data to be displayed on the liquid crystal displaying section;

a liquid crystal driver that retrieves the display-data stored in the single-port memory on a specific cycle and sends the display-data to the liquid crystal displaying section; and

a controller that controls the liquid crystal driver so that, when a CPU does not have access to the single-port memory, the display-data is retrieved from the single-port memory to the liquid crystal driver on the specific cycle and the retrieved data is sent to the liquid crystal displaying section, whereas,

when the CPU has access to the single-port memory while the data is being retrieved from the single-port memory to the liquid crystal driver, a priority is given to the CPU so that the CPU starts an access operation while the liquid crystal driver stops a display-data retrieval operation, and on completion of the access operation, the liquid crystal driver starts again the display-data retrieval operation.

20. A liquid crystal display apparatus having a semiconductor device for driving liquid crystals and a liquid crystal displaying section, the device comprising:

a single-port memory that stores display-data to be displayed on the liquid crystal displaying section;

a liquid crystal driver, having a latch circuit that stores the display-data stored in the single-port memory, that retrieves the display-data from the single-port memory on a specific cycle and sends the display-data to the liquid crystal displaying section; and

a controller that generates a latch control signal and sends the latch control signal to the latch circuit, the latch control signal being generated based on a CPU-access signal indicating an access operation of a CPU to the single-port memory and a specific signal that is synchronized with a display-data retrieval cycle for the liquid crystal driver.